WHAT IS CLAIMED IS:

1. A method comprising:

sending bits of data on an input line and on a control line of a test access protocol (TAP) controller of a JTAG-compliant device; and

receiving and storing the bits of data from the input line and from the control line at the TAP controller.

2. The method of Claim 1, wherein the receiving and storing are performed in response to the TAP controller being in a shift data register state or a pause data register state.

3. The method of Claim 1, wherein the receiving and storing are performed in response to a burst-write instruction being an active instruction in the TAP controller.

4. The method of Claim 3, further comprising loading the burst-write instruction into an instruction register of the TAP controller.

5. The method of Claim 1, further comprising receiving and storing bits in response to:

the TAP controller being in an Exit1 data register state, and

a burst-write instruction being an active instruction in the TAP controller.

6. The method of Claim 1, further comprising receiving and storing bits in response to:

the TAP controller being in an Exit2 data register state, and

a burst-write instruction being an active instruction in the TAP controller.

7. The method of Claim 1, wherein the storing the bits comprises shifting the bits into a least significant bit of a data register.

8. An apparatus comprising:

a JTAG-compliant test access protocol (TAP) controller;

a control (TMS) line connected to the TAP controller; and

an input (TDI) line connected to the TAP controller,

the control and input lines adapted to transmit data bits, and

the TAP controller adapted to receive and store the data bits transmitted on the control and input lines.

9. The apparatus of Claim 8, wherein the TAP controller is adapted to receive the data bits in response to the TAP controller being in a shift data register (Shift-data-register) state or a pause data register (Pause-data-register) state.

10. The apparatus of Claim 8, wherein the TAP controller is adapted to receive the data bits in response to a burst-write instruction being an active instruction in the TAP controller.

11. The apparatus of Claim 8, further comprising a data register accessible by the TAP controller, the data register adapted to store the data bits received from the control line and from the input line.

12. The apparatus of Claim 11, wherein the data register is adapted to store the data bits by shifting the data bits into a least significant bit of the data register.

13. The apparatus of Claim 8, wherein the TAP controller is adapted to receive the data bits of in response to:

the TAP controller being in an Exit1 data register state, and

a burst-write instruction being an active instruction in the TAP controller.

14. The apparatus of Claim 8, wherein the TAP controller is adapted to receive the data bits of in response to:

the TAP controller being in an Exit2 data register state, and

a burst-write instruction being an active instruction in the TAP controller.

15. A computer program product stored on a computer operable media, the computer program product comprising software code effective to:

send bits of data on an input line and on a control line of a test access protocol (TAP) controller of a JTAG-compliant device; and

receive and store the bits of data from the input line and from the control line at the TAP controller.

16. The computer program product of Claim 15, wherein the software code effective to receive and store are each performed in response to the TAP controller being in a shift data register state or a pause data register state.

17. The computer program product of Claim 15, wherein the software code effective to receive and store are each performed in response to a burst-write instruction being an active instruction in the TAP controller.

18. The computer program product of Claim 17, further comprising software code effective to load the burst-write instruction into an instruction register of the TAP controller.

19. The computer program product of Claim 15, further comprising software code effective to receive and store the data bits in response to:

the TAP controller being in an Exit1 data register state, and

a burst-write instruction being an active instruction in the TAP controller.

20. The computer program product of Claim 15, further comprising software code effective to receive and store the data bits in response to:

the TAP controller being in an Exit2 data register state, and

a burst-write instruction being an active instruction in the TAP controller.

21. The computer program product of Claim 15, wherein the software code effective to store the bits comprises software code effective to shift the bits into a least significant bit of a data register.